# HITACHI IC MEMORIES
## HM4716A / AP ( -1 / -2 / -3 / -4 )

HITACHI

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### 16384-word × 1-bit Dynamic Random Access Memory

The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe $(\overline{CE})$. Data out of the HM4716A will remain valid from the access time from the Column Address Strobe unitl $\overline{CE}$ goes into precharge (logic 1). However, in early write cyles ($\overline{W}$ active low before $\overline{CE}$ goes low), the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data well remain valid at the output during a read cycle from TCELQV until $\overline{CE}$ returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both $\overline{CE}$ and/or $\overline{RE}$ can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2ms by either of the two following methods:

(1) normal read or write cycles on 128 addresses, A0 to A6.

(2) $\overline{RE}$ only cycles on 128 addresses, A0 to A6.

A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

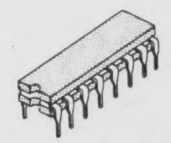
$\overline{RE}$ only regreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.

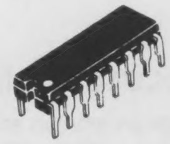
| Old | New | Definitions |
|---|---|---|
| A0-A6 | A0-A6 | Address Inputs |
| $\overline{CAS}$ | $\overline{CE}$ | Column Address Strobe |
| $D_{IN}$ | D | Data In |
| $D_{OUT}$ | Q | Data Out |
| $\overline{RAS}$ | $\overline{RE}$ | Row Address Strobe |
| $\overline{WRITE}$ | $\overline{W}$ | Read/Write Input |
| $V_{BB}$ | VBB | Power (−5V) |
| $V_{CC}$ | VCC | Power (+5V) |
| $V_{DD}$ | VDD | Power (+12V) |
| $V_{SS}$ | VSS | Ground |

**HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4**



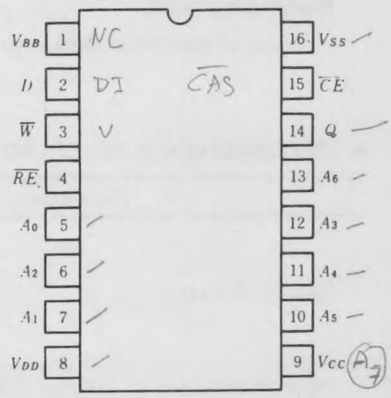
**(DG-16A)**

**HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4**



**(DP-16)**

■ **PIN ARRANGEMENT**



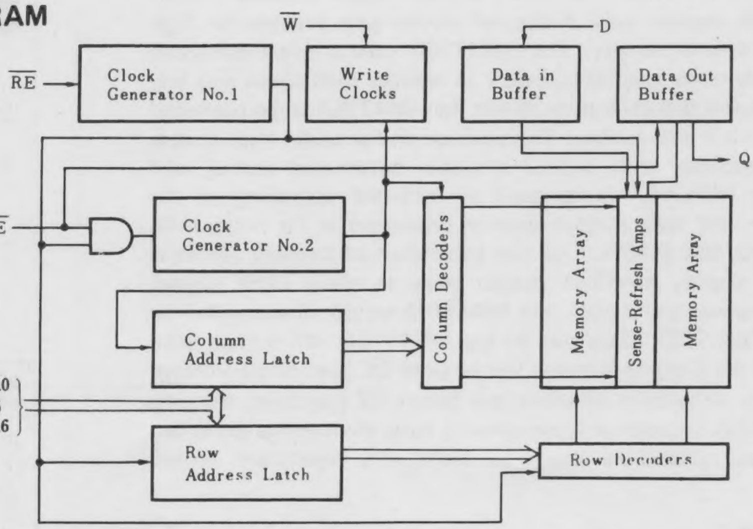

(Top View)

## ■ FEATURES

- All Inputs Including Clocks TTL Compatible
- Input Latches for Address and Data in
- Three-State TTL Compatible Output
- Common I/O Capability
- Only 128 Refresh Cycles Required Every 2ms
- Standard Power Supplies +12V, +5V, −5V (all with 10% tolelance)

- Maximum Access Time
  - HM4716A-1 .......... 120ns
  - HM4716A-2 ............ 150ns
  - HM4716A-3 ............ 200ns
  - HM4716A-4 ............ 250ns
- Read or Write Cycle Time
  - HM4716A-1 .......... 320ns
  - HM4716A-2 ............ 320ns
  - HM4716A-3 ............ 375ns
  - HM4716A-4 ............ 410ns

## ■ FUNCTIONAL DIAGRAM




## ■ ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Voltage on any pin relative to VBB .................. | −0.5V to+20V |
| Voltage on VDD, VCC Supplies relative to VSS ......... | −0.5V to +15V |
| Voltage on Q pin relative to VSS .................. | −0.5V to +10V |
| Operating Temperature, TA (Ambient) .............. | 0°C to +70°C |
| Storage Temperature (Ambient)* ..................... | −65°C to +150°C |
| Short-circuit output current ...................... | 50mA |
| Power dissipation ............................. | 1W |

* In case of HM4716AP Series are −55°C to +125°C.

## ■ RECOMMENDED DC OPERATING CONDITIONS (TA=0 to +70℃)

| Parameter | Symbol | min. | typ. | max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | 10.8 | 12.0 | 13.2 | V | 1 |
| | VCC | 4.5 | 5.0 | 5.5 | V | |
| | VSS | 0 | 0 | 0 | V | |
| | VBB | −4.5 | −5.0 | −5.5 | V | |
| Input High (logic 1) Voltage $\overline{RE}$, $\overline{CE}$, $\overline{W}$ | VIHC | 2.7 | — | 6.5 | V | 1 |
| Input High (logic 1) Voltage All inputs except $\overline{RE}$, $\overline{CE}$, $\overline{W}$ | VIH | 2.4 | — | 6.5 | V | 1 |
| Input Low (logic 0) Voltage all inputs | VIL | −1.0 | — | 0.8 | V | 1 |

## ■ DC ELECTRICAL CHARACTERISTICS (TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VBB=−5V±10%, VSS=0V)

| Parameter | Symbol | min. | max. | Units | Notes |
|---|---|---|---|---|---|
| OPERATING CURRENT | IDD1 | — | 35 | mA | 2 |
| Average Power Supply Operating Current | ICC1 | — | — | mA | 3 |
| ($\overline{RE}$, $\overline{CE}$ Cycling; TRELREL=375ns) | IBB1 | — | 300 | μA | 2 |
| STANDBY CURRENT | IDD2 | — | 1.5 | mA | |
| Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ = VIHC) | ICC2 | −10 | 10 | μA | 5 |
| | IBB2 | — | 100 | μA | |
| REFRESH CURRENT | IDD3 | — | 27 | mA | 2 |
| Average Power Supply Current, Refresh Mode | ICC3 | −10 | 10 | μA | 5 |
| ($\overline{RE}$ Cycling, $\overline{CE}$=VIHC; TRELREL=375ns) | IBB3 | — | 300 | μA | 2 |
| PAGE MODE CURRENT | IDD4 | — | 27 | mA | |
| Average Power Supply Current, Page-mode Operation | ICC4 | — | — | mA | 3 |
| ($\overline{RE}$=VIL, $\overline{CE}$ Cycling; TCELCEL=225ns) | IBB4 | — | 300 | μA | |
| INPUT LEAKAGE<br>Input Leakage Current, any Input (VBB=−5V, VIN=0 to +7V, all other pins not under test=0V) | IIL | −10 | 10 | μA | |
| OUTPUT LEAKAGE<br>Output Leakage Current (Q is Disabled, VOUT=0 to +5.5V) | IOL | −10 | 10 | μA | 5 |
| OUTPUT LEVELS<br>Output High (Logic 1) Voltage (IOUT=−5mA) | VOH | 2.4 | VCC | V | 4 |
| Output Low (Logic 0) Voltage (IOUT=4.2mA) | VOL | 0 | 0.4 | V | |

NOTES

1. All voltages referenced to VSS, VBB must be applied before and removed after other supply voltage.
2. Current depend on cycle rate: maximum current is measured at the fastest cycle rate.
3. ICC depends upon output loading. The VCC supply is connected to the output buffer only.
4. Output voltage will swing from VSS to VCC when activated with no current loading. For purposes of maintaining data in standby mode, VCC may be reduced to VSS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.
5. ICC2, ICC3 and IOL consists of leakage current only.
6. AC measurements assume TT = 5ns.
7. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIHC or VIH and VIL.
8. Assumes that TRELCEL = TRELCEL (max). If TRELCEL is greater than the maximum recommended value shown in this table, TRELQV exceeds the value shown.
9. Assumes that TRELCEL = TRELCEL (max).
10. Measured with a load circuit equivalent to 2TTL loads and 100pF (in case of HM4716A-2:1 TTL and 50pF). And VSS + 0.8V, VSS + 2.0V are the reference level for measuring timing of Q.
11. TCEHQZ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation with the TRELCEL (max) limit insures that TRELQC (max) can be met TRELCEL (max) is specified as a reference point only; if TRELCEL is greater than the specified TRELCEL (max) limit, then access time is controlled exclusively by TCELQV.
13. These parameters are referenced to $\overline{CE}$ leading edge in early write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
14. TWLCEL, TCELWL and TRELWL are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if TWLCEL = TWLCEL (min), the cycle is an early write and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if TCELWL = TCELWL (min) and TRELWL will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Capacitance measured with Boonton Meter or effective capacitance measuring method.
16. $\overline{CE}$ = VIHC to disable Q.

## ■ AC ELECTRICAL CHARACTERISTICS

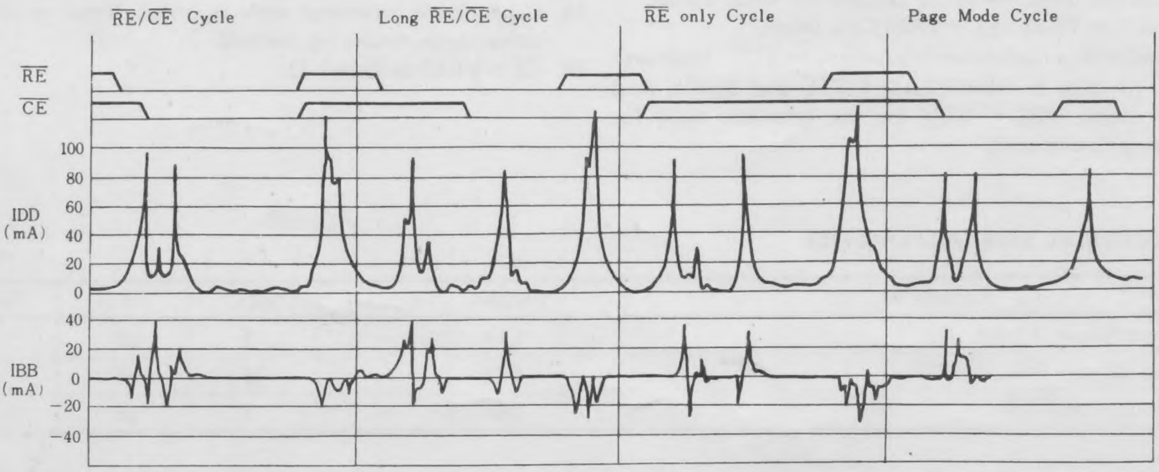
| Parameter | Symbol | typ. | max. | Units | Notes |
|---|---|---|---|---|---|
| Input Capacitance (A0-A6, D) | CI1 | — | 5 | pF | 15 |
| Input Capacitance $\overline{RE}$, $\overline{CE}$, $\overline{W}$ | CI2 | — | 10 | pF | 15 |
| Output Capacitance (Q) | CQ | — | 7 | pF | 15, 16 |

## ■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(TA=0 to +70°C, VDD=12V±10%, VCC=5V±10%, VSS=0V, VBB=−5V±10%)

| Parameter | Symbol | | HM4716A-1 | | HM4716A-2 | | HM4716A-3 | | HM4716A-4 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Old | New | min. | max. | min. | max. | min. | max. | min. | max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | TRELREL | 320 | – | 320 | – | 375 | – | 410 | – | ns | |
| Read-Write Cycle Time | $t_{RWC}$ | TRELREL | 320 | – | 320 | – | 375 | – | 515 | – | ns | |
| Page Mode Cycle Time | $t_{PC}$ | TCELCEL | 160 | – | 170 | – | 225 | – | 275 | – | ns | |
| Access Time From $\overline{RE}$ | $t_{RAC}$ | TRELQV | – | 120 | – | 150 | – | 200 | – | 250 | ns | 8, 10 |
| Access Time From $\overline{CE}$ | $t_{CAC}$ | TCELQV | – | 80 | – | 100 | – | 135 | – | 165 | ns | 9, 10 |
| Output Buffer Turn-off Delay | $t_{OFF}$ | TCEHQZ | 0 | 35 | 0 | 50 | 0 | 60 | 0 | 70 | ns | 11 |
| Transition Time (Rise and Fall) | $t_T$ | TT | 3 | 35 | 3 | 35 | 3 | 50 | 3 | 50 | ns | 7 |
| $\overline{RE}$ Precharge Time | $t_{RP}$ | TREHREL | 100 | – | 100 | – | 120 | – | 150 | – | ns | |
| $\overline{RE}$ Pulse Width | $t_{RAS}$ | TRELREH | 120 | 10000 | 150 | 10000 | 200 | 10000 | 250 | 10000 | ns | |
| $\overline{RE}$ Hold Time | $t_{RSH}$ | TCELREH | 80 | – | 100 | – | 135 | – | 165 | – | ns | |
| $\overline{CE}$ Pulse Width | $t_{CAS}$ | TCELCEH | 80 | 10000 | 100 | 10000 | 135 | 10000 | 165 | 10000 | ns | |
| $\overline{CE}$ Hold Time | $t_{CSH}$ | TRELCEH | 120 | – | 150 | – | 200 | – | 250 | – | ns | |
| $\overline{RE}$ to $\overline{CE}$ Delay Time | $t_{RCD}$ | TRELCEL | 15 | 40 | 25 | 50 | 30 | 65 | 40 | 85 | ns | 12 |
| CE to RE Precharge Time | $t_{CRP}$ | TCEHREL | 0 | – | −20 | – | −20 | – | −20 | – | ns | |
| Row Address Set-up Time | $t_{ASR}$ | TAVREL | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Row Address Hold Time | $t_{RAH}$ | TRELAX | 15 | – | 20 | – | 25 | – | 35 | – | ns | |
| Column Address Set-up Time | $t_{ASC}$ | TAVCEL | −5 | – | −5 | – | −5 | – | −5 | – | ns | |
| Column Address Hold Time | $t_{CAH}$ | TCELAX | 40 | – | 45 | – | 55 | – | 75 | – | ns | |
| Column Address Hold Time Reference to $\overline{RE}$ | $t_{AR}$ | TRELAX | 80 | – | 95 | – | 120 | – | 160 | – | ns | |
| Read Command Set-up Time | $t_{RCS}$ | TWHCEL | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Read Command Hold Time | $t_{RCH}$ | TCEHWL | 0 | – | 20 | – | 20 | – | 20 | – | ns | |
| Write Command Hold Time | $t_{WCH}$ | TCELWH | 40 | – | 45 | – | 55 | – | 75 | – | ns | |
| Write Command Hold Time Referenced $\overline{RE}$ | $t_{WCR}$ | TRELWH | 80 | – | 95 | – | 120 | – | 160 | – | ns | |
| Write Command Pulse Width | $t_{WP}$ | TWLWH | 40 | – | 45 | – | 55 | – | 75 | – | ns | |
| Write Command to $\overline{RE}$ Lead Time | $t_{RWL}$ | TWLREH | 50 | – | 60 | – | 80 | – | 100 | – | ns | |
| Write Command to $\overline{CE}$ Lead Time | $t_{CWL}$ | TWLCEH | 50 | – | 60 | – | 80 | – | 100 | – | ns | |
| Data-in Set-up Time | $t_{DS}$ | TDVCEL | 0 | – | 0 | – | 0 | – | 0 | – | ns | 13 |
| Data-in Hold Time | $t_{DH}$ | TCELDX | 40 | – | 45 | – | 55 | – | 75 | – | ns | 13 |
| Data-in Hold Time Referenced $\overline{RE}$ | $t_{DHR}$ | TRELDX | 80 | – | 95 | – | 120 | – | 160 | – | ns | |
| $\overline{CE}$ Precharge Time (for Page-mode Cycle Only) | $t_{CP}$ | TCEHCEL | 60 | – | 60 | – | 80 | – | 100 | – | ns | |
| Refresh Period | $t_{REF}$ | TRVRV | – | 2 | – | 2 | – | 2 | – | 2 | ms | |
| $\overline{W}$ Command Set-up Time | $t_{WCS}$ | TWLCEL | 0 | – | −20 | – | −20 | – | −20 | – | ns | 14 |
| $\overline{CE}$ to $\overline{RE}$ Delay | $t_{CWD}$ | TCELWL | 60 | – | 70 | – | 95 | – | 125 | – | ns | 14 |
| $\overline{RE}$ to $\overline{W}$ Delay | $t_{RWD}$ | TRELWL | 100 | – | 120 | – | 160 | – | 200 | – | ns. | 14 |
| $\overline{RE}$ Precharge to $\overline{CE}$ Hold Time | $t_{RPC}$ | TREHCEL | 0 | – | 0 | – | 0 | – | 0 | – | ns | |

## ■ CURRENT WAVEFORMS

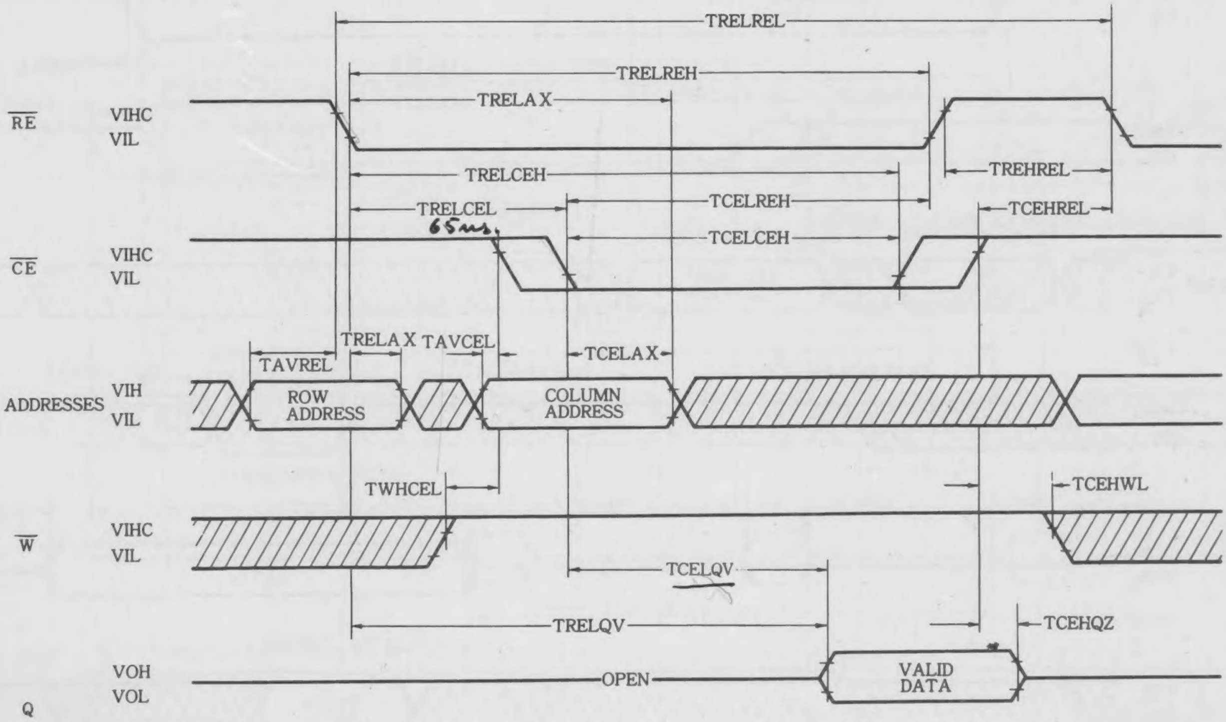



NOTE : VDD=13.2V, VBB=−4.5V, Ta=25°C

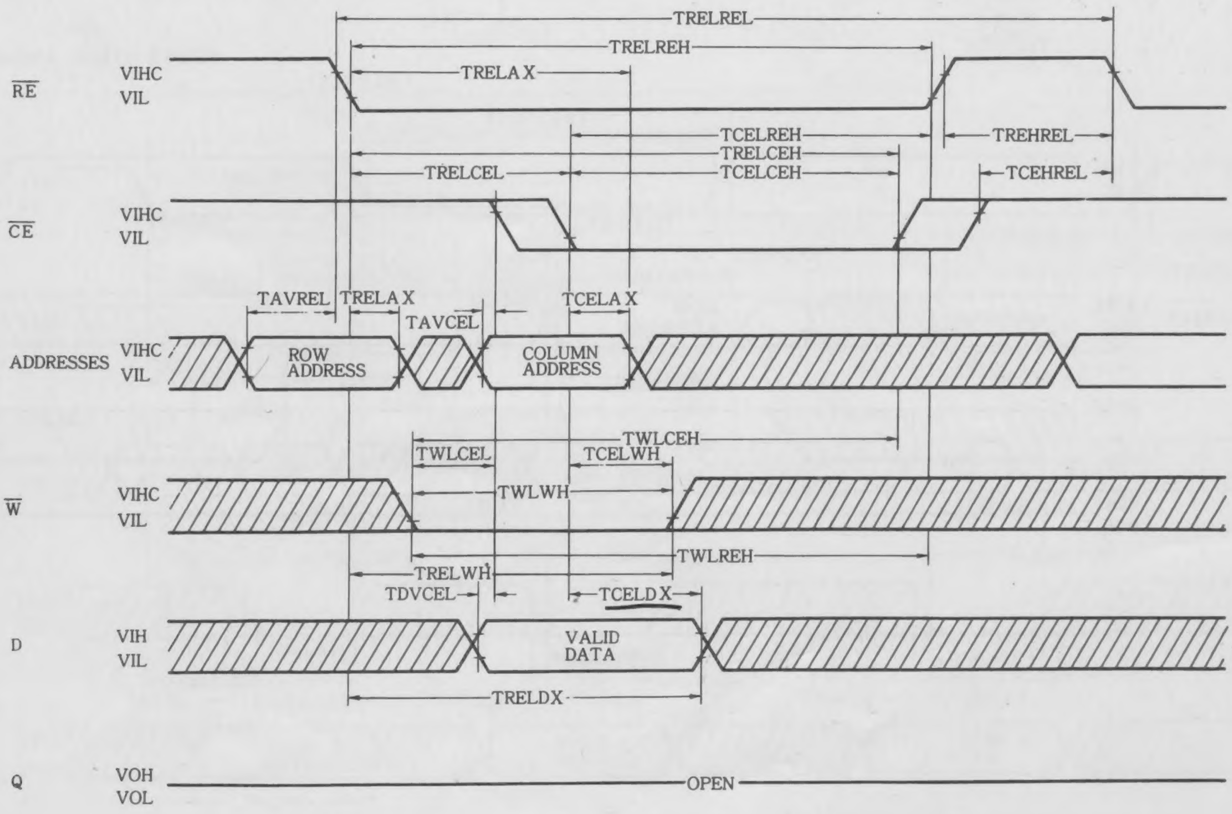
50ns

## ■ TIMING WAVEFORMS

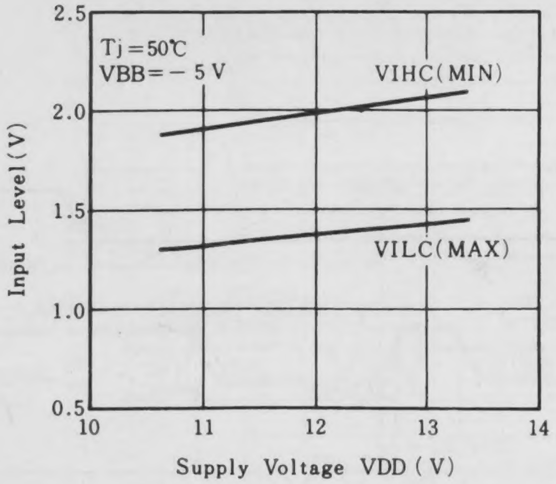
### • READ CYCLE



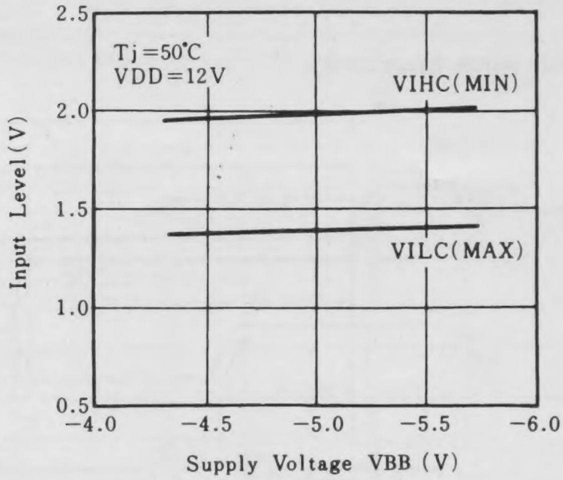

### • WRITE CYCLE (EARLY WRITE)



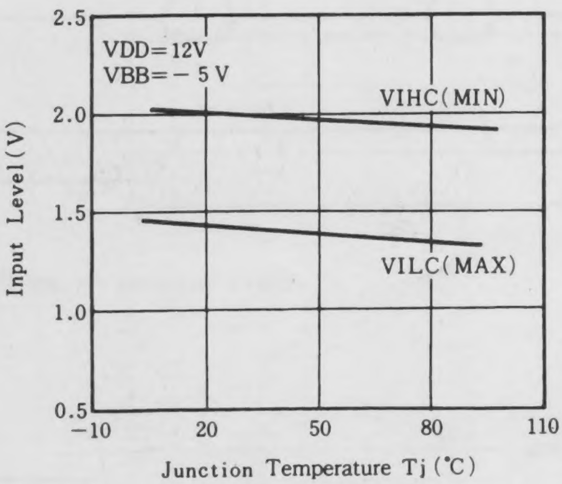
**CLOCK INPUT LEVELS vs. VDD**



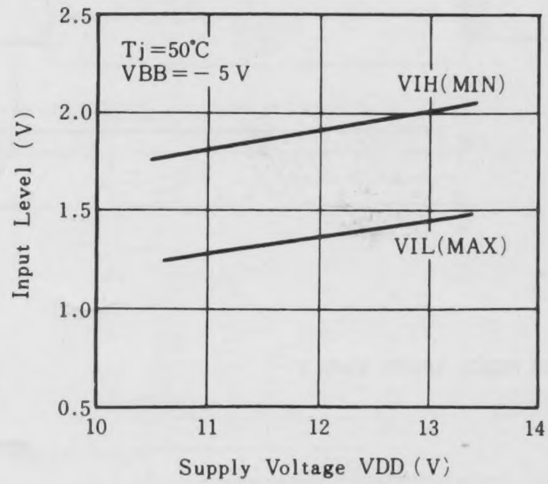

**CLOCK INPUT LEVELS vs. VBB**



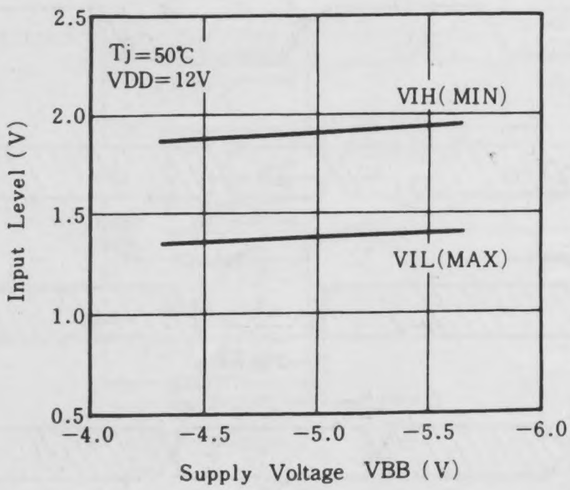

**CLOCK INPUT LEVELS vs. Tj**



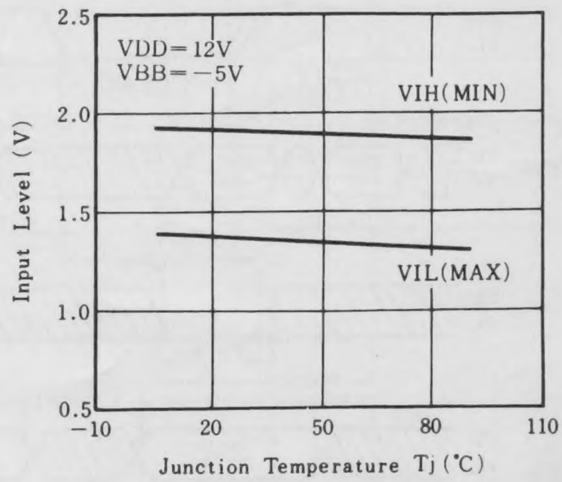

**ADDRESS AND DATA INPUT LEVELS vs. VDD**




**ADDRESS AND DATA INPUT LEVELS vs. VBB**




**ADDRESS AND DATA INPUT LEVELS vs. Tj**





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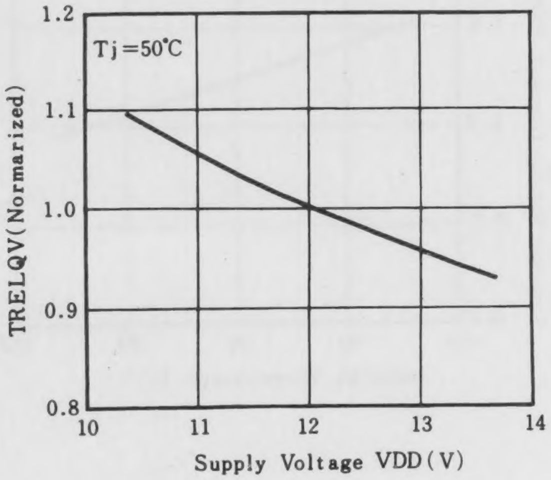
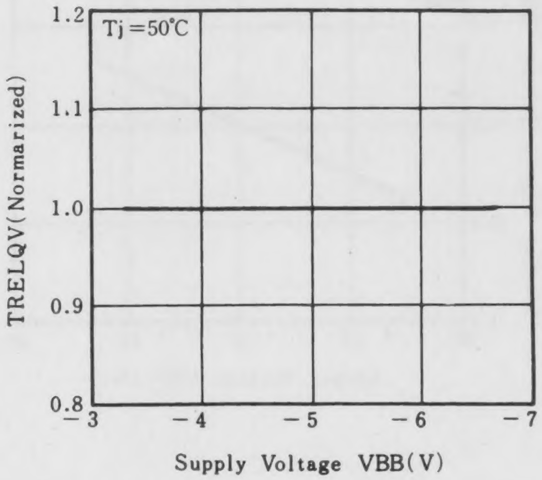
## ■ TYPICAL CHARACTERISTICS

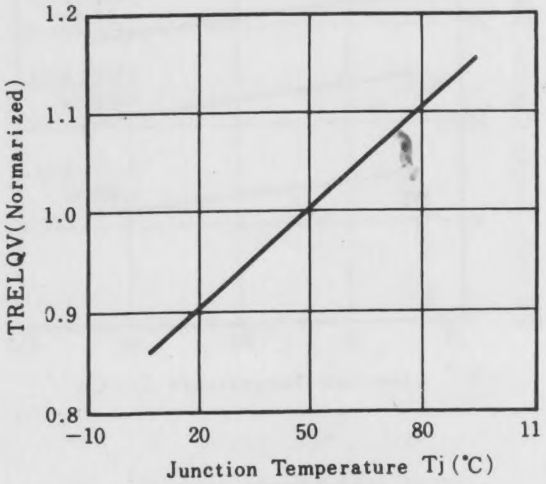
### ACCESS TIME (NORMARIZED) vs. VDD



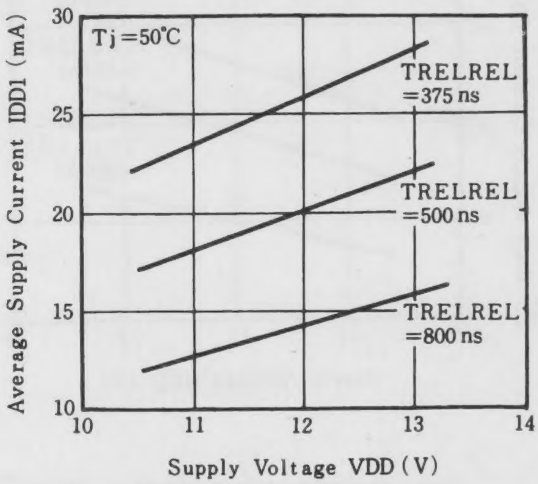

### ACCESS TIME (NORMARIZED) vs. $V_{BB}$



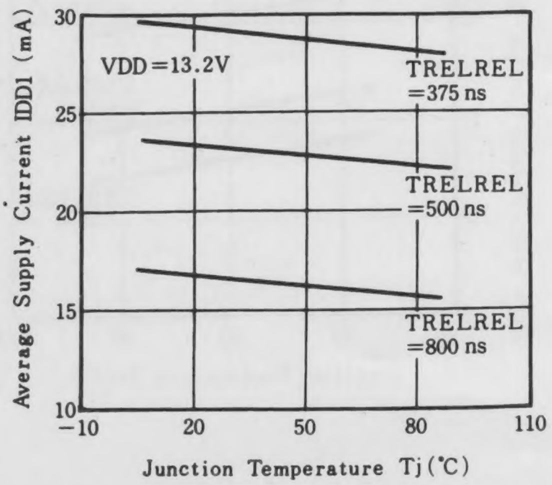

### ACCESS TIME (NORMARIZED ) vs. Tj



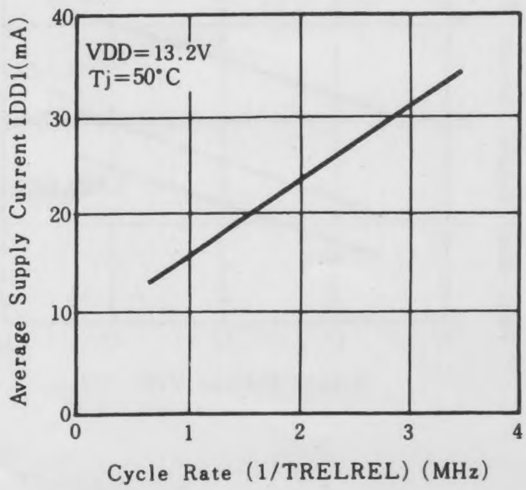

### IDDI vs. $V_{DD}$



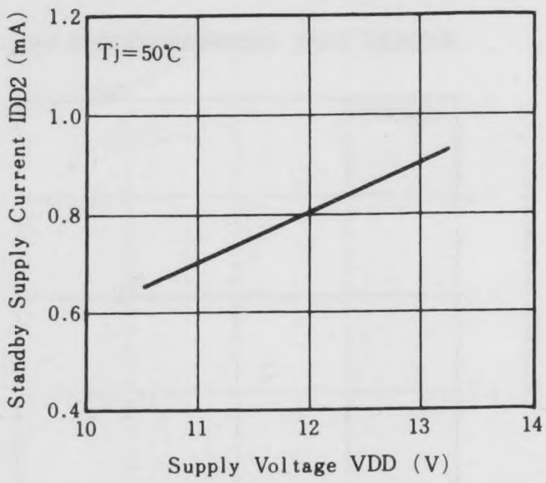

### IDDI vs. Tj



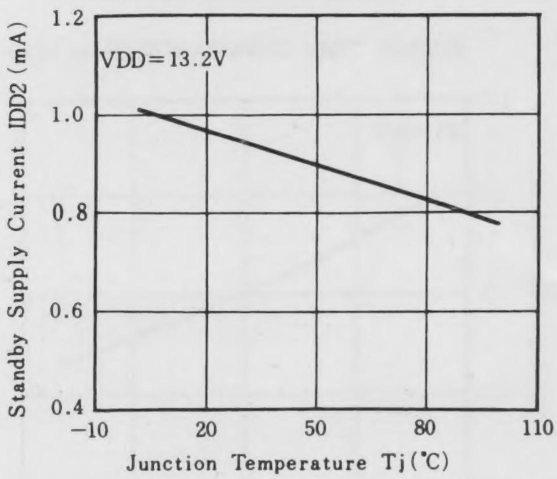

### IDDI vs. CYCLE RATE



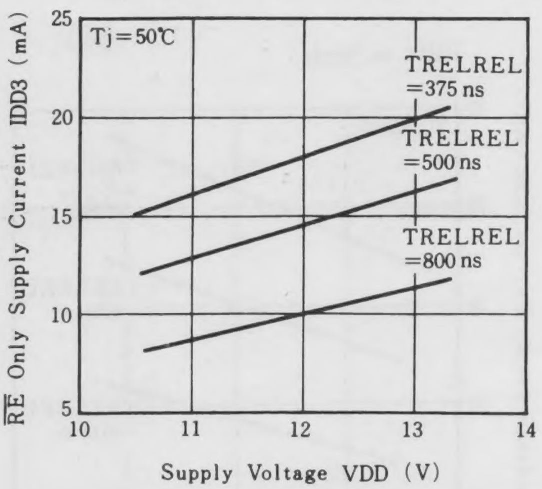
IDD2 (STANDBY) vs. VDD



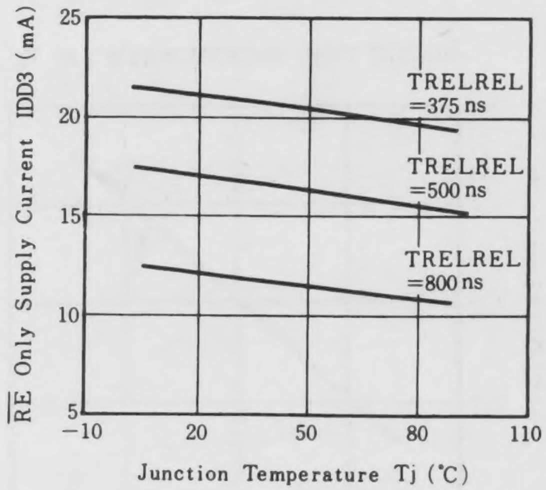

IDD2 (STANDBY) vs. Tj



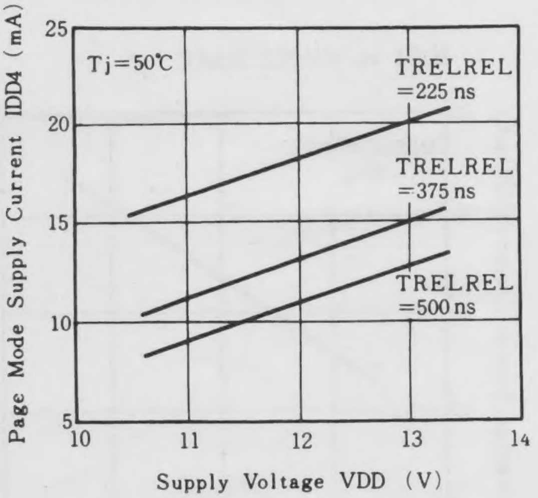

IDD3 ($\overline{RE}$ ONLY CYCLE) vs. VDD



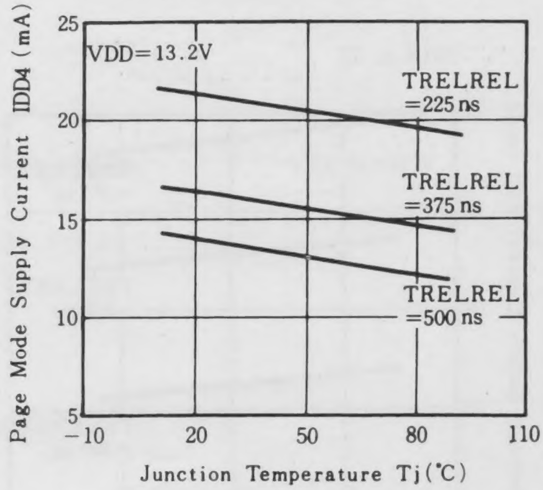

IDD3 ($\overline{RE}$ ONLY CYCLE) vs. Tj




IDD4 (PAGE-MODE CYCLE) vs. VDD




IDD4 (PAGE-MODE CYCLE) vs. Tj

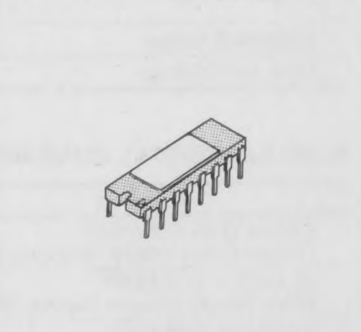


# HITACHI IC MEMORIES
## HM4864 ( −2 / −3 )

HITACHI

### 65536-word X 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.
This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.
In addition to the usual read, write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{\text{RAS}}$-only refresh.
Proper control of the clock inputs ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

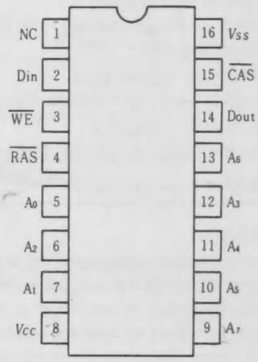


(DC-16)

### ■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle (HM4864-2)
  200ns access time, 335ns cycle (HM4864-3)
- Single power supply of +5V±10% with a built-in $V_{BB}$ generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{\text{CAS}}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{\text{RAS}}$-only refresh, and Page-mode capability
- 128 refresh cycle

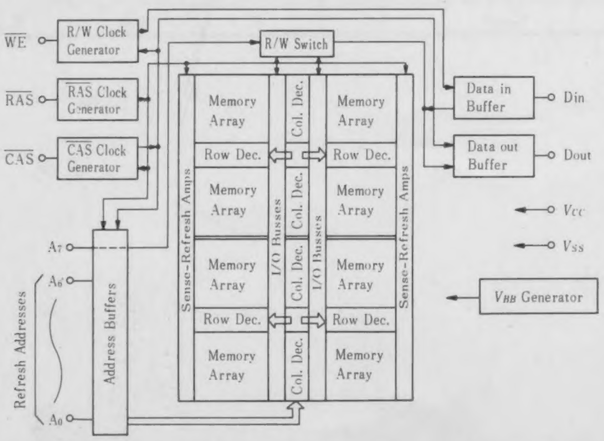
### ■ PIN ARRANGEMENT




(Top View)

| | |
|---|---|
| $A_0$-$A_7$ | Address Inputs |
| $\overline{\text{CAS}}$ | Column Address Strobe |
| Din | Data In |
| Dout | Data Out |
| $\overline{\text{RAS}}$ | Row Address Strobe |
| $\overline{\text{WE}}$ | Read/Write Input |
| $V_{CC}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| $A_0$-$A_6$ | Refresh Address Strobe |

### ■ FUNCTIONAL DIAGRAM






Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

## ■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to $V_{SS}$ . . . . . . . . . . . . . . . . . . . . . . . . . −1.0 to +7V
Operating Temperature, Ta (Ambient) . . . . . . . . . . . . . . . . . . . . . . 0 to +70°C
Storage Temperature (Ambient) . . . . . . . . . . . . . . . . . . . . . . −65 to +150°C
Short-circuit Output Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 50 mA
Power Dissipation . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1 W

## ■ RECOMMENDED DC OPERATING CONDITIONS ($T_a$ = 0 to +70°C)

| Parameter | Symbol | min. | typ. | max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | 1 |
| | $V_{SS}$ | 0 | 0 | 0 | V | |
| Input High Voltage | $V_{IH}$ | 2.4 | – | 6.5 | V | 1 |
| Input Low Voltage | $V_{IL}$ | −1.0 | – | 0.8 | V | 1 |

## ■ DC ELECTRICAL CHARACTERISTICS ($T_a$ = 0 to +70°C, $V_{CC}$ = 5V±10%, $V_{SS}$ = 0V)

| Parameter | Symbol | min. | max. | Unit | Notes |
|---|---|---|---|---|---|
| OPERATING CURRENT<br>Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC}$=min.) | $I_{CC1}$ | – | 60 | mA | 2, 4 |
| STANDBY CURRENT<br>Power Supply Standby Current ($\overline{RAS}$ = $V_{IH}$, $D_{out}$ = High Impedance) | $I_{CC2}$ | – | 3.5 | mA | |
| REFRESH CURRENT<br>Average Power Supply Current, Refresh Mode<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ = $V_{IH}$; $t_{RC}$ = min.) | $I_{CC3}$ | – | 4.5 | mA | |
| PAGE MODE CURRENT<br>Average Power Supply Current, Page-mode Operation<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ Cycling; $t_{PC}$ = min.) | $I_{CC4}$ | – | 45 | mA | 4 |
| INPUT LEAKAGE<br>Input Leakage Current, any Input ($V_{in}$ = 0 to +6.5V, all other pins not under test = 0V) | $I_{IL}$ | −10 | 10 | μA | |
| OUTPUT LEAKAGE<br>Output Leakage Current ($D_{out}$ is disabled, $V_{out}$ = 0 to +5.5V) | $I_{OL}$ | −10 | 10 | μA | 3 |
| OUTPUT LEVELS<br>Output High (Logic 1) Voltage ($I_{out}$ = −5mA) | $V_{OH}$ | 2.4 | $V_{CC}$ | V | |
| Output Low (Logic 0) Voltage ($I_{out}$ = 4.2mA) | $V_{OL}$ | 0 | 0.4 | V | |

NOTES
1. All voltages referenced to $V_{SS}$.
2. $I_{CC}$ depends on output loading condition when the device is selected. $I_{CC}$ max. is specified at the output open condition.
3. $I_{OL}$ consists of leakage current only.
4. Current depends on cycle rate: maximum current is measured at the fastest cycle rate.

## ■ AC ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | typ. | max. | Unit | Notes |
|---|---|---|---|---|---|
| Input Capacitance ($A_0$-$A_7$, $D_{in}$) | $C_{in1}$ | – | 7 | pF | 1 |
| Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) | $C_{in2}$ | – | 10 | pF | 1 |
| Output Capacitance ($D_{out}$) | $C_{out}$ | – | 7 | pF | 1, 2 |

NOTES
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = $V_{IH}$ to disable Dout.

## ■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[1), 2)]

($T_a$ = 0 to +70°C, $V_{CC}$ = 5V±10%, $V_{SS}$ = 0V)

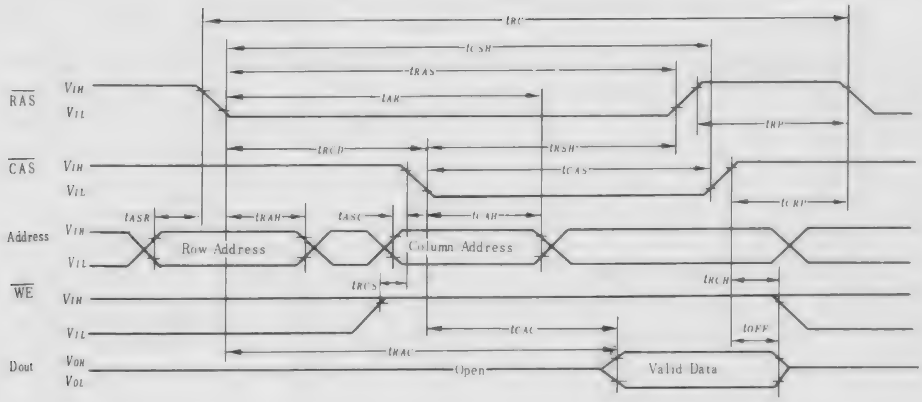
| Parameter | Symbol | HM4864-2 | | HM4864-3 | | Unit | Notes |
|---|---|---|---|---|---|---|---|
| | | min. | max. | min. | max. | | |
| Random Read or Write Cycle Time | $t_{RC}$ | 270 | – | 335 | – | ns | |
| Read-Write Cycle Time | $t_{RWC}$ | 270 | – | 335 | – | ns | |
| Page Mode Cycle Time | $t_{PC}$ | 170 | – | 225 | – | ns | |
| Access Time from $\overline{RAS}$ | $t_{RAC}$ | – | 150 | – | 200 | ns | 4, 6 |
| Access Time from $\overline{CAS}$ | $t_{CAC}$ | – | 100 | – | 135 | ns | 5, 6 |
| Output Buffer Turn-off Delay | $t_{OFF}$ | 0 | 40 | 0 | 50 | ns | 7 |
| Transition Time (Rise and Fall) | $t_T$ | 3 | 35 | 3 | 50 | ns | 3 |
| $\overline{RAS}$ Precharge Time | $t_{RP}$ | 100 | – | 120 | – | ns | |
| $\overline{RAS}$ Pulse Width | $t_{RAS}$ | 150 | 10000 | 200 | 10000 | ns | |
| $\overline{RAS}$ Hold Time | $t_{RSH}$ | 100 | – | 135 | – | ns | |
| $\overline{CAS}$ Pulse Width | $t_{CAS}$ | 100 | – | 135 | – | ns | |
| $\overline{CAS}$ Hold Time | $t_{CSH}$ | 150 | – | 200 | – | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay Time | $t_{RCD}$ | 20 | 50 | 25 | 65 | ns | 8 |
| $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $t_{CRP}$ | −20 | – | −20 | – | ns | |
| Row Address Set-up Time | $t_{ASR}$ | 0 | – | 0 | – | ns | |
| Row Address Hold Time | $t_{RAH}$ | 20 | – | 25 | – | ns | |
| Column Address Set-up Time | $t_{ASC}$ | −10 | – | −10 | – | ns | |
| Column Address Hold Time | $t_{CAH}$ | 45 | – | 55 | – | ns | |
| Column Address Hold Time referenced to $\overline{RAS}$ | $t_{AR}$ | 95 | – | 120 | – | ns | |
| Read Command Set-up Time | $t_{RCS}$ | 0 | – | 0 | – | ns | |
| Read Command Hold Time | $t_{RCH}$ | 0 | – | 0 | – | ns | |
| Write Command Hold Time | $t_{WCH}$ | 45 | – | 55 | – | ns | |
| Write Command Hold Time referenced to $\overline{RAS}$ | $t_{WCR}$ | 95 | – | 120 | – | ns | |
| Write Command Pulse Width | $t_{WP}$ | 45 | – | 55 | – | ns | |
| Write Command to $\overline{RAS}$ Lead Time | $t_{RWL}$ | 45 | – | 55 | – | ns | |
| Write Command to $\overline{CAS}$ Lead Time | $t_{CWL}$ | 45 | – | 55 | – | ns | |
| Data-in Set-up Time | $t_{DS}$ | 0 | – | 0 | – | ns | 9 |
| Data-in Hold Time | $t_{DH}$ | 45 | – | 55 | – | ns | 9 |
| Data-in Hold Time referenced to $\overline{RAS}$ | $t_{DHR}$ | 95 | – | 120 | – | ns | |
| $\overline{CAS}$ Precharge Time (for Page-mode Cycle Only) | $t_{CP}$ | 60 | – | 80 | – | ns | |
| Refresh Period | $t_{REF}$ | – | 2 | – | 2 | ms | |
| $\overline{WE}$ Command Set-up Time | $t_{WCS}$ | −20 | – | −20 | – | ns | 10 |
| $\overline{CAS}$ to $\overline{RAS}$ Delay | $t_{CWD}$ | 60 | – | 80 | – | ns | 10 |
| $\overline{RAS}$ to $\overline{WE}$ Delay | $t_{RWD}$ | 110 | – | 145 | – | ns | |
| $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time | $t_{RPC}$ | 0 | – | 0 | – | ns | |

NOTES

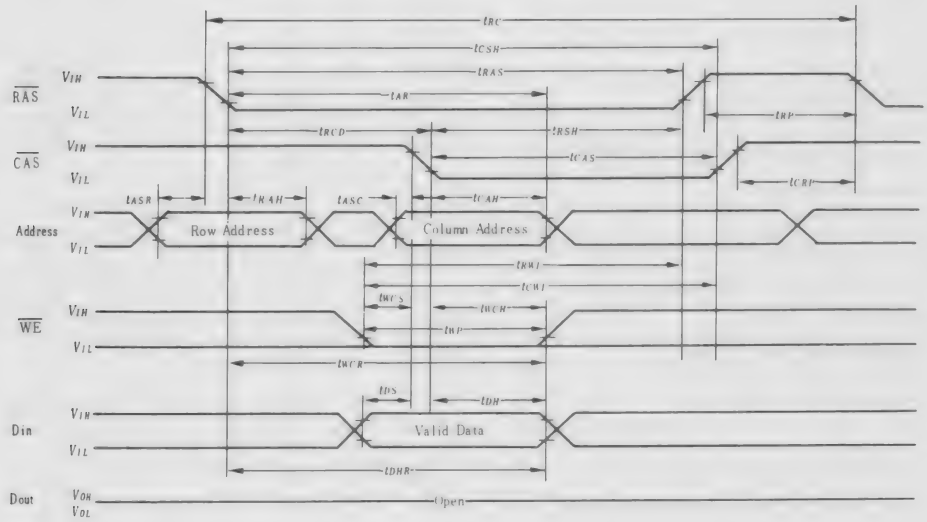
1. AC measurements assume $t_T$ = 5ns.
2. 8 cycles are required after power-on or prolonged periods (greater than 2ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
3. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
4. Assumes that $t_{RCD}$ = $t_{RCD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
5. Assumes that $t_{RCD}$ = $t_{RCD}$ (max).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively be $t_{CAC}$.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cyeles.
10. $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS}$ = $t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD}$ = $t_{CWD}$ (min) and $t_{RWD}$ = $t_{RWD}$ (min) the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

## ■ TIMING WAVEFORMS

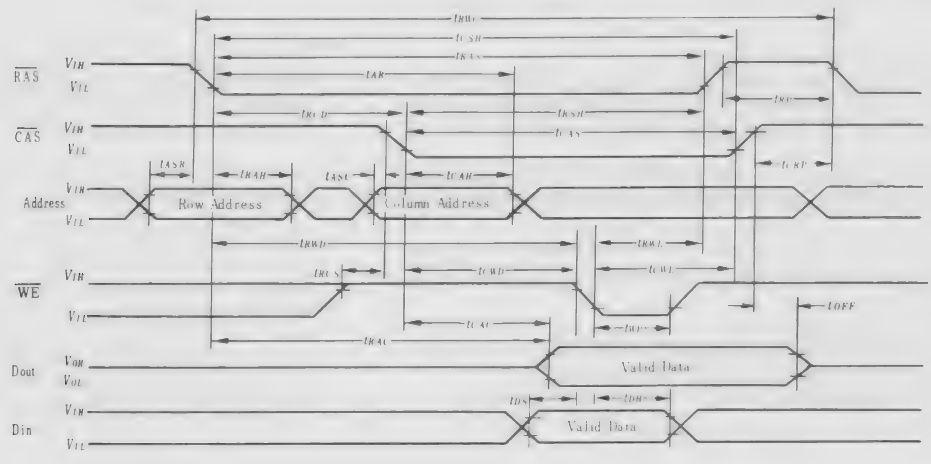
### • READ CYCLE



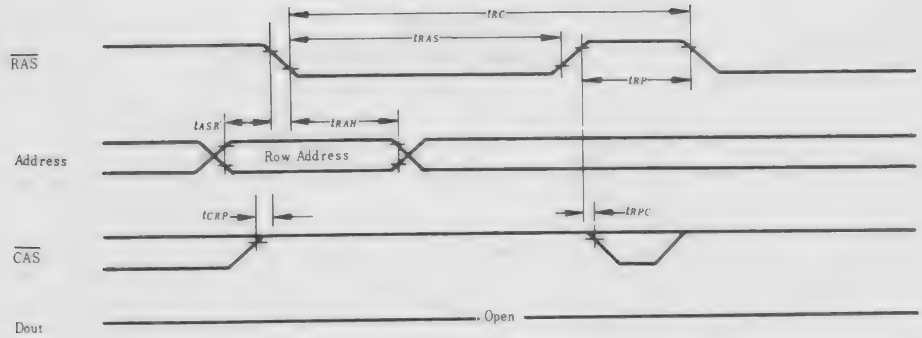

### • WRITE CYCLE



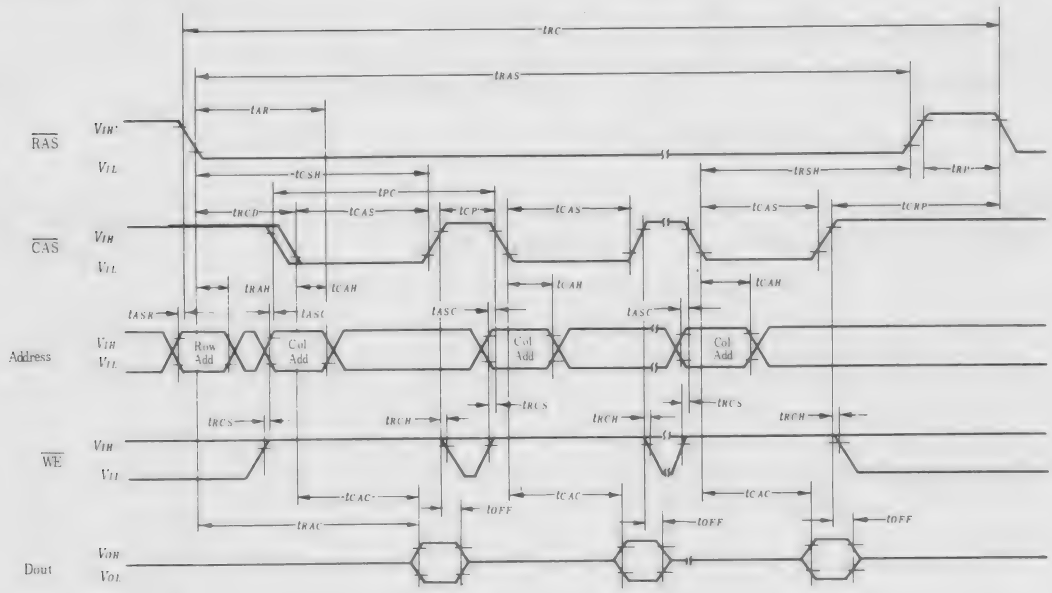

### • READ-WRITE/READ-MODIFY-WRITE CYCLE



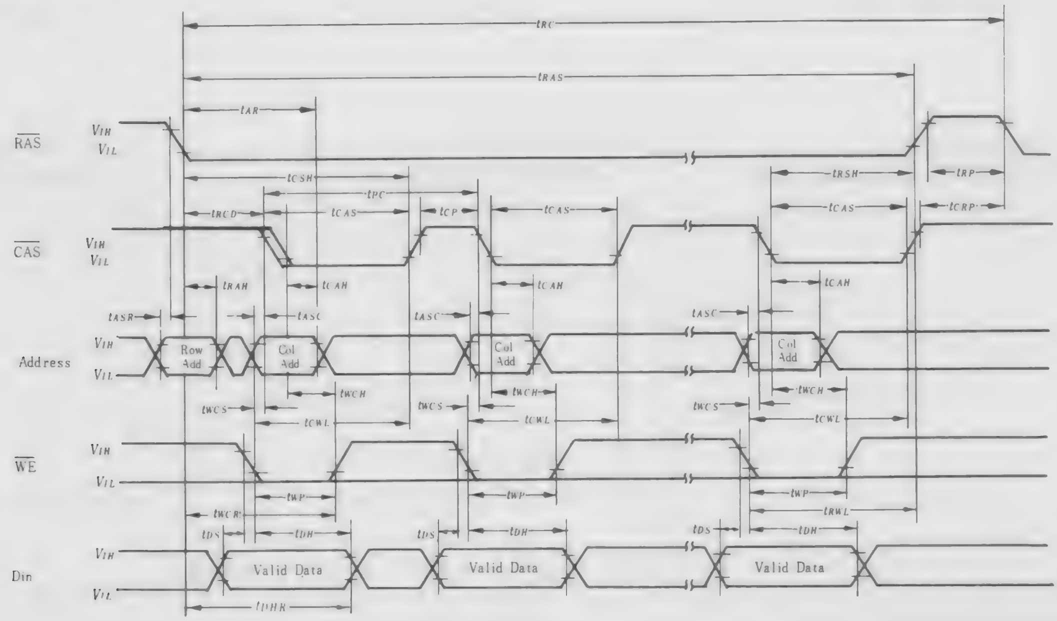
- **"$\overline{RAS}$-ONLY" REFRESH CYCLE**



- **PAGE MODE READ CYCLE**

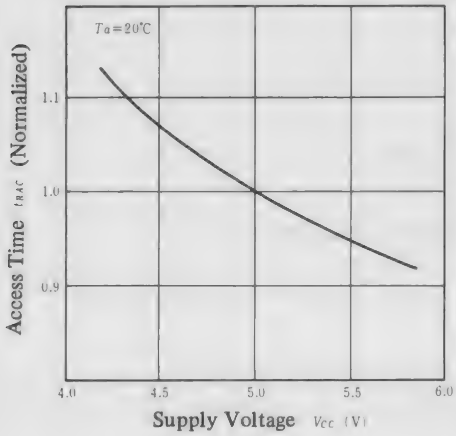


- **PAGE MODE WRITE CYCLE**

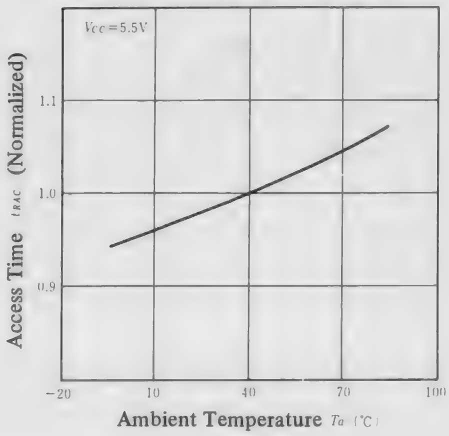


■ **TYPICAL CHARACTERISTICS**

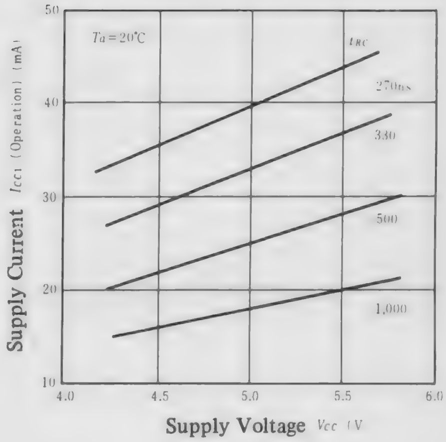
### ACCESS TIME vs. SUPPLY VOLTAGE



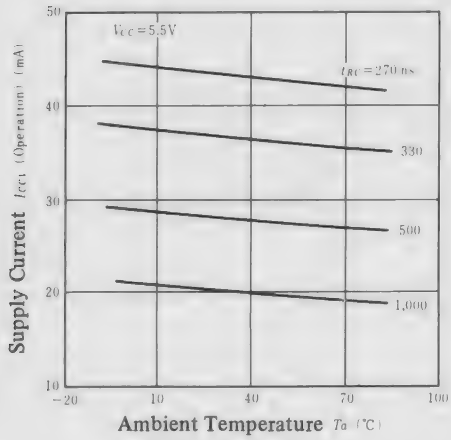

### ACCESS TIME vs. AMBIENT TEMPERATURE



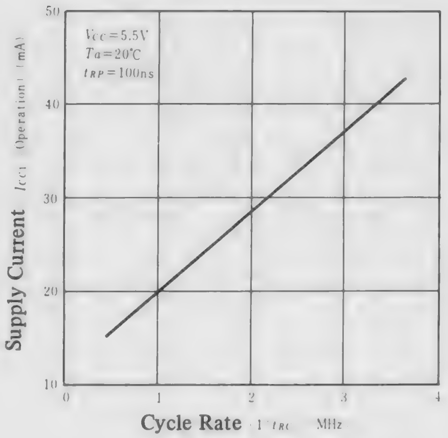

### SUPPLY CURRENT vs. SUPPLY VOLTAGE



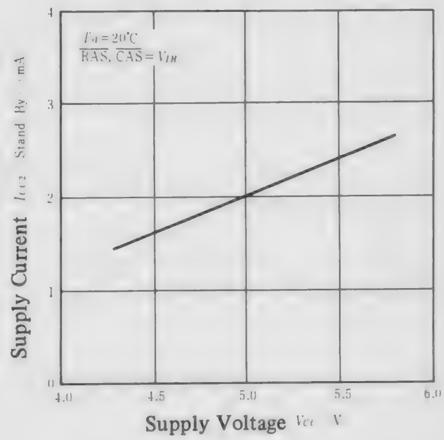

### SUPPLY CURRENT vs. AMBIENT TEMPERATURE



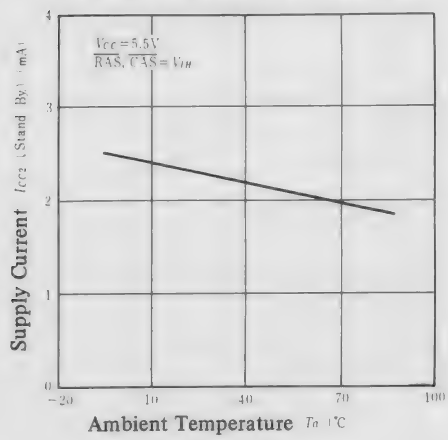

### SUPPLY CURRENT vs. CYCLE RATE



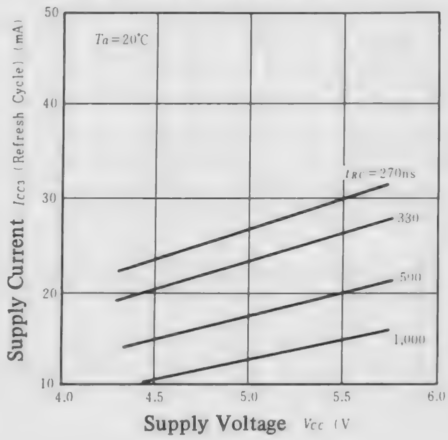

### SUPPLY CURRENT vs. SUPPLY VOLTAGE



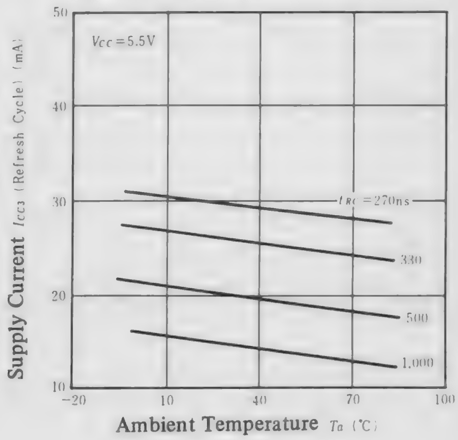

### SUPPLY CURRENT vs. AMBIENT TEMPERATURE



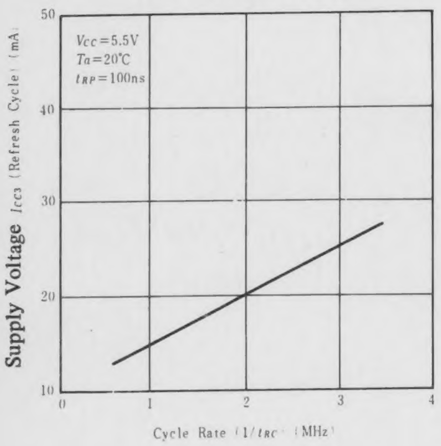

### SUPPLY CURRENT vs. SUPPLY VOLTAGE



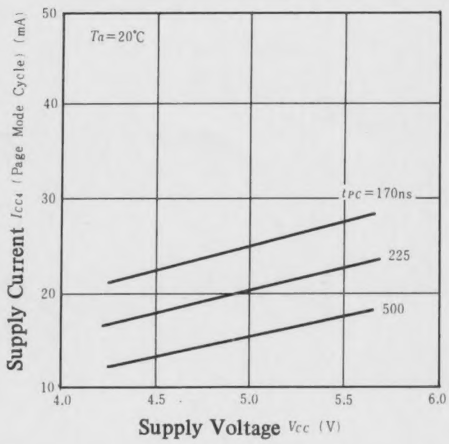

### SUPPLY CURRENT vs. AMBIENT TEMPERATURE



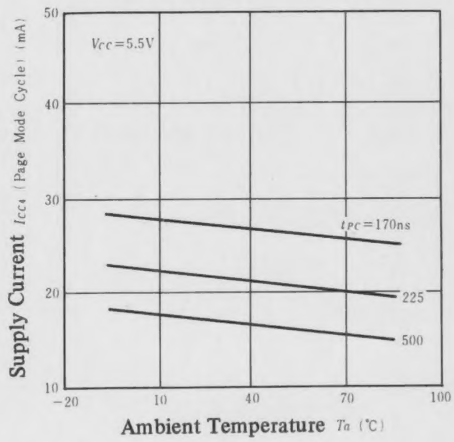
### SUPPLY CURRENT vs. CYCLE RATE



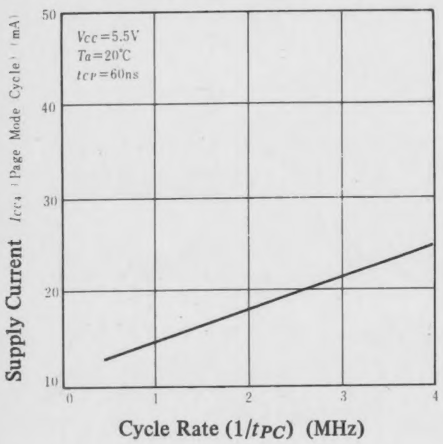

### SUPPLY CURRENT vs. SUPPLY VOLTAGE



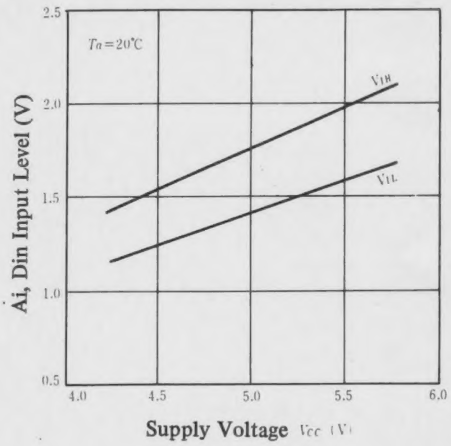

### SUPPLY CURRENT vs. AMBIENT TEMPERATURE



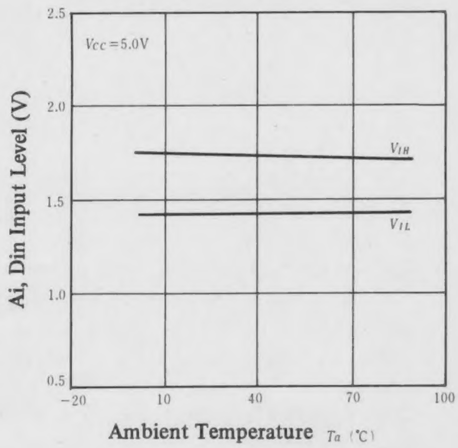

### SUPPLY CURRENT vs. CYCLE RATE



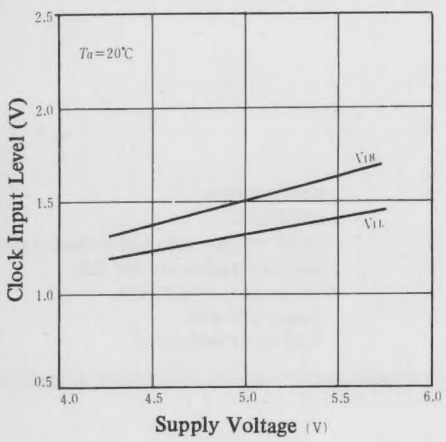

### INPUT LEVEL vs. SUPPLY VOLTAGE



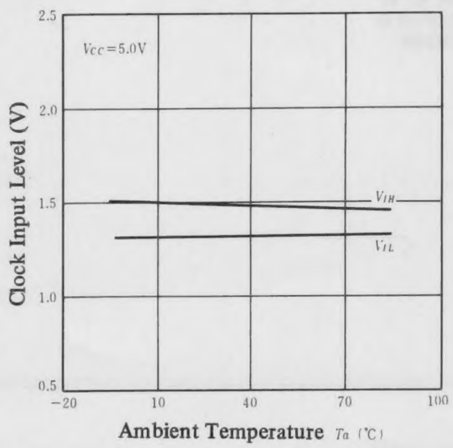

### INPUT LEVEL vs. AMBIENT TEMPERATURE

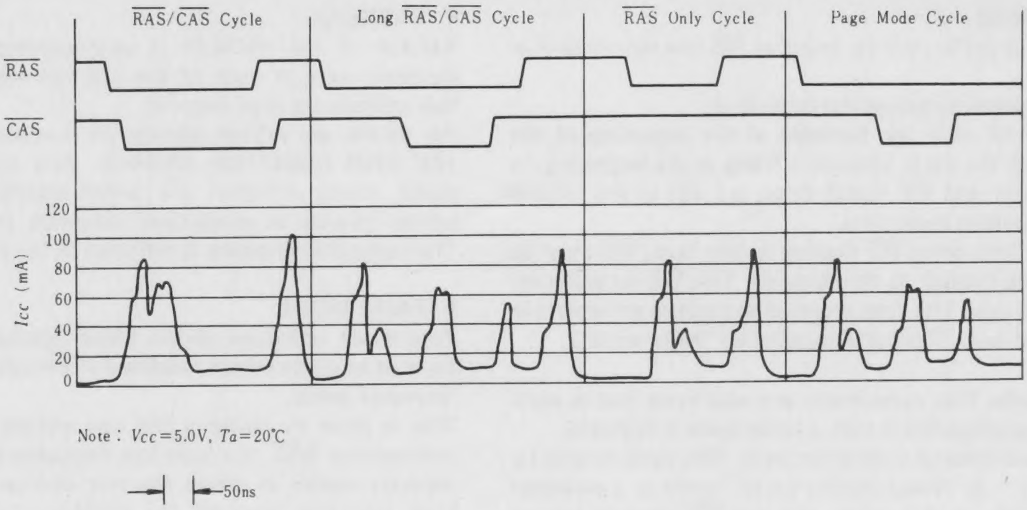



### CLOCK INPUT LEVEL vs. SUPPLY VOLTAGE




### CLOCK INPUT LEVEL vs. AMBIENT TEMPERATURE






## ■ APPLICATION INFORMATION

### ● POWER ON

An initial pause of 500 μs is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation.

The $V_{CC}$ current ($I_{CC}$) requirement of the HM4864 during power on is, however, dependent upon the input levels ($\overline{RAS}$, $\overline{CAS}$) and the rise time of $V_{CC}$, as shown in Fig. 1.

### ● READ CYCLE

A read cycle begins with addresses stable and a negative going transition of $\overline{RAS}$. The time delay between the stable address and the start of $\overline{RAS}$-on is controlled by parameter $t_{ASR}$.

Following the time when $\overline{RAS}$ reaches its low level, the row address must be held stable long enough to be captured. This controlling parameter is $t_{RAH}$. Following this interval, the address can be changed from row address to column address. When the column address is stable, $\overline{CAS}$ can be turned on. The leading edge of $\overline{CAS}$ is controlled by parameter $t_{RCD}$. The basic limit on the $\overline{CAS}$ leading edge is that $\overline{CAS}$ can not start untill the column address is stable, and this is controlled by parameter $t_{ASC}$. The column address must be held stable long enough to be captured. The controlling parameter is $t_{CAH}$.

Note that $t_{RCD}$ (max) is not an operating limit of the HM4864 though its specification is listed on the data sheets. If $\overline{CAS}$ becomes on later than $t_{RCD}$ (max), the access time from $\overline{RAS}$ will be increase by the time which $t_{RCD}$ exceeds $t_{RCD}$ (max).

Following the time when $\overline{CAS}$ reaches its low level, the data-out pin remains in a high impedance state until a valid data appears. This parameter is $t_{CAC}$-access time from $\overline{CAS}$.

The access time from $\overline{RAS}$-$t_{RAC}$-is the time from $\overline{RAS}$-on to valid Dout.

The minimum value of $t_{RAC}$ is derived as the sum of $t_{RCD}$ (max) and $t_{CAC}$.

The selected output data is held valid internally until $\overline{CAS}$ becomes high, and then Dout pin becomes high impedance. This parameter is $t_{OFF}$.

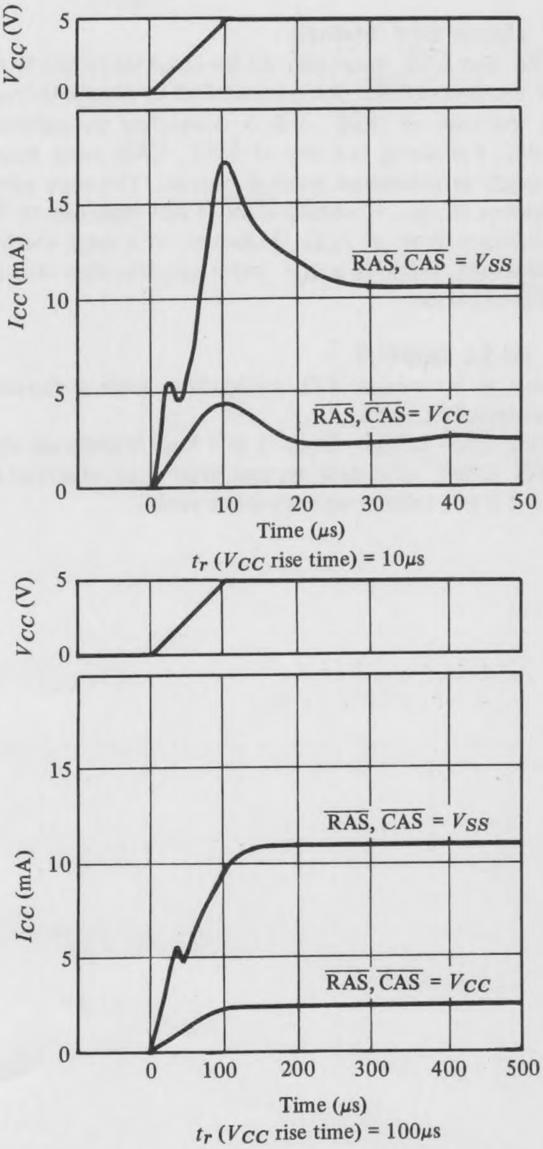



**Fig. 1 Typical $I_{CC}$ vs. $V_{CC}$ during power up.**

- **WRITE CYCLE**

A write cycle is performed by bringing $\overline{\mathrm{WE}}$ low before or during $\overline{\mathrm{CAS}}$-on.

Two different write cycles can be defined as;

Write cycle-Write data are available at the beginning of the $\overline{\mathrm{CAS}}$-on so that the write operation starts at the beginning. In this mode, Dout and $\overline{\mathrm{WE}}$ signal times are not in any critical path for determining cycle time.

Following the time when $\overline{\mathrm{WE}}$ reaches its low level, $\overline{\mathrm{WE}}$ must be held stable long enough to be captured. This $\overline{\mathrm{WE}}$-on pulse deration is called $t_{WP}$. The time required to capture write data in a latch is called $t_{DH}$. This cycle is called an "early write".

Read Write cycle- This cycle starts as a read cycle, but as soon as the device specification is met, a write cycle is initiated. $\overline{\mathrm{WE}}$ and Din are delayed until after Dout. This cycle is called a "delayed write". A "Read-modify-write" cycle is a variation of this operation. In this mode, Din and $\overline{\mathrm{WE}}$ become critical path signals for determining cycle time.

- **CLOCK-OFF TIMING**

$\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ must stay on for Dout stabilized to valid data. In the case of $\overline{\mathrm{CAS}}$, this is controlled by parameter $t_{CAS}$ (min). In the case of $\overline{\mathrm{RAS}}$, this is controlled by parameter $t_{RSH}$ (min). Following the end of $\overline{\mathrm{RAS}}$, $\overline{\mathrm{CAS}}$ must stay off long enough to precharge internal circuits. The only parameter of concern is $t_{RP}$. Normally $\overline{\mathrm{CAS}}$ is not required to be off for minimum time of $t_{CRP}$. However, in a page mode memory operation, there is a $t_{CP}$ (min) specification to control the $\overline{\mathrm{CAS}}$-off time.

- **DATA OUTPUT**

Dout is three-state TTL compatible with a fan-out of two standard TTL loads.

When $\overline{\mathrm{CAS}}$ is high, Dout is in a high impedance state. When $\overline{\mathrm{CAS}}$ is low, valid data appears after $t_{CAC}$ at a read cycle, and Dout is not valid at an early-write cycle.

- **REFRESH**

Refresh of the HM4864 is accomplished by performing a memory cycle at each of the 128 row addresses within each two millisecond time interval.

A0 to A6 are refresh address pin compatible with standard 16K RAM (HM4716A, HM4816). Any cycle in which $\overline{\mathrm{RAS}}$ signal occurs refreshes the entire selected row. $\overline{\mathrm{RAS}}$-only refresh results in substantial reduction in operating power. This reduction in power is reflected in the $I_{CC3}$ specification.

- **PAGE MODE**

Page mode operation allows faster successive memory operations at multiple colum locations of the same row address with increased speed.

This is done by strobing the row address into the chip and maintaining $\overline{\mathrm{RAS}}$ at a logic low throughout all successive $\overline{\mathrm{CAS}}$ memory cycles in which the row address is latched. As the time normally required for strobing a new row address is eliminated, access and cycle times can be decreased and the operating power is reduced. These are specifications.

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